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AF/2800 #22

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Thakur et al.	§	Group Art Unit:	2815
Serial No.:	09/654,093	§	Examiner:	P. Brock II
Filed:	August 31, 2000	§	Atty. Docket:	94-0302.02
For: A METHOD TO AVOID THRESHOLD VOLTAGE SHIFT IN THICKER DIELECTRIC FILMS		§		

PETITION PURSUANT TO 37 C.F.R. §1.181(a) REQUESTING WITHDRAWAL OF THE HOLDING OF ABANDONMENT

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2/26/04 Susan Jerome
Date Signature

Dear Sir:

Pursuant to 37 C.F.R. §1.181(a), Applicants hereby petition to request withdrawal of the holding of abandonment. A brief statement of the facts follow.

Claims 52-64 are pending and were rejected by the Examiner. The sole reasons for rejecting independent claim 60 were based on §112 and §103. (See Board Decision at p. 2-3. A copy of the Board Decision is included in an appendix to this Petition.) The sole reasons for rejecting claim 60's dependent claims 61-64 were based on §103. (***Id.*** at p. 3, 22.) Significantly, the Examiner failed to reject dependent claims 61-64 under the same §112 basis cited against their independent claim 60. (***Id.*** at p. 2-3, 22.) Applicants appealed claims 52-64. As part of the appeal, Applicants argued against the express rejections specified above. The Board affirmed the §112 rejection against claim 60 but reversed all §103 rejections against claims 60-64. (***Id.*** at p. 23.) The Board further suggested that the Examiner reopen prosecution in order to reject dependent claims 61-64 under the same §112 basis cited against their independent claim 60. (***Id.*** at p. 22.)

On December 30, 2003, Applicants received a copy of the Board Decision. After careful review of the Board Decision, relevant statutes, rules, and MPEP guidelines,

Applicants believed a direct response by Applicants to the Board Decision would be improper. Accordingly, Applicants awaited an action from the Examiner.

On February 24, 2004, during a telephone conversation with the Examiner, the Examiner indicated a belief that an Examiner response to the Board Decision was not warranted and that Applicants should have responded to the Board Decision. The Examiner refused to reopen prosecution and deemed the application to be abandoned. The Examiner also admitted an unfamiliarity with the post-Board decision process.

Applicants contend that with the Board's reversal of every express rejection against claims 61-64, there exists a post-Board decision circumstance addressed in MPEP §1214.06 II. MPEP §1214.06 addresses situations where the Board sustains the Examiner in whole or in part, and part II specifies the situation where claims stand allowed. The first sentence under part II expresses that "[t]he appellant is not required to file a reply" and requires the Examiner to take appropriate action. Alternatively, Applicants contend that the Board's decision is relevant to part III, which addresses situations wherein the Board affirms in part but also reverses a rejection that brings certain claims up for an action on the merits. Part III announces that the Examiner "*will* take up the application . . . for appropriate action on the matters thus brought up." (Emphasis added.)

During the February 24, 2004 telephone conversation with the Examiner, the Examiner argued that the Board effectively rejected claims 61-64 under §112, thereby leaving no claims standing allowed. Applicants contend that a careful reading of the relevant portion of the Board's decision (page 22) demonstrates that the Board specifically refrained from raising such a rejection and instead urged the Examiner to address the matters brought up for action on the merits.

Accordingly, Applicants request that the Commissioner find that the above-captioned application is not abandoned and instead awaits an action from the Examiner on the merits. In the interest of efficient prosecution Applicants are concurrently submitting an amendment that should place the application in condition for allowance. Specifically, Applicants are amending the claims to avoid the existing §112 rejection as

well as other §112 rejections foreseen by the Board. Applicants are also canceling claims 52-59, whose rejections were upheld by the Board.

Applicants understand that no fee is due.

Please address further correspondence with this application to: Charles B. Brantley, II, Micron Technology, Inc., Mail Stop 525, 8000 S. Federal Way, Boise, ID 83706-9632, telephone number (208) 368-4557.

MICRON, TECHNOLOGY, INC.

2/26/4

Charles Brantley

Charles B. Brantley II, Reg. No. 38-086

Appendix

Board Decision

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RANDHIR P.S. THAKUR, RAVI IYER and HOWARD RHODES

Appeal No. 2003-2155
Application 09/654,093

ON BRIEF

Before OWENS, WALTZ and LIEBERMAN, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal is from the final rejection of claims 52-64, which are all of the claims pending in the application.

THE INVENTION

The appellants claim methods for processing a semiconductor device. Claim 52 is illustrative:

52. A method of processing a semiconductor device, comprising:

depositing a dielectric layer over a semiconductor substrate, said substrate comprising a plurality of electrically conductive regions and an electrically insulative region therebetween;

allowing electrically chargeable particles to occur in said dielectric layer;

allowing some diffusion of said electrically chargeable particles; and

preventing at least some of said electrically chargeable particles from reaching said substrate.

THE REFERENCES

Van Der Scheer et al. (Van Der Scheer)	4,976,856	Dec. 11, 1990
Boland et al. (Boland)	5,084,407	Jan. 28, 1992
Ghezzi et al. (Ghezzi)	5,132,239	Jul. 21, 1992
Doan et al. (Doan)	5,372,974	Dec. 13, 1994
Ying	5,384,288	Jan. 24, 1995
Cunningham et al. (Cunningham)	5,468,689	Nov. 21, 1995

THE REJECTIONS

Claim 60 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The claims stand rejected under 35 U.S.C. § 103 as follows: claim 52 over Doan in view of Boland;

claims 53-57 over Doan in view of Cunningham; claims 58 and 59 over Doan in view of Cunningham and Ying; claims 60, 61, 63 and 64 over Doan in view of Ghezzi; and claim 62 over Doan in view of Ghezzi and Van Der Scheer.

OPINION

We affirm the rejection under 35 U.S.C. § 112, second paragraph, and the rejections under 35 U.S.C. § 103 of claim 52 over Doan in view of Boland, claims 53-57 over Doan in view of Cunningham, and claims 58 and 59 over Doan in view of Cunningham and Ying. We reverse the rejections of claims 60, 61, 63 and 64 over Doan in view of Ghezzi, and claim 62 over Doan in view of Ghezzi and Van Der Scheer.

The appellants state that with respect to the rejections under 35 U.S.C. § 103, claims 60-64 stand or fall separately and claims 52-59 stand or fall in the following groups: 1) claim 52, 2) claims 53-57, and 3) claims 58 and 59 (brief, page 3).[1] We therefore limit our discussion of the rejections of claims 52-59 to claim 52 and one claim in each of the other groups, i.e., claims 53 and 59. *See In re Ochiai*, 71 F.3d 1565, 1566 n.2,

[1] Citations herein to the brief are to the second brief (filed November 25, 2002). Because the arguments in the reply brief are similar to those in the brief, we limit our discussion to the brief.

37 USPQ2d 1127, 1129 n.2 (Fed. Cir. 1995); 37 CFR § 1.192(c)(7)(1997).

Rejection under 35 U.S.C. § 112, second paragraph

When a word of degree such as "substantially" is used in a claim, the specification must provide some standard for measuring that degree such that one of ordinary skill in the art would understand what is claimed when the claim is read in light of the specification. *See Seattle Box Co. v. Industrial Crating & Packing, Inc.*, 731 F.2d 818, 826, 221 USPQ 568, 573-74 (Fed. Cir. 1984).

The appellants' figure 1 provides some standard for measuring the degree encompassed by "generally laterally coextensive" with respect to lead 16 and insulating region 14. The appellants' disclosure, however, provides no standard for measuring the degree encompassed by "generally insulative material" and "generally conductive material".

The appellants' specification does not define "generally". Hence, we give this term its ordinary meaning, *see Allen Engineering Corp. v. Bartell Industries Inc.*, 299 F.3d 1336, 1344, 63 USPQ2d 1769, 1772 (Fed. Cir. 2002), which is: "**1**. with respect to the larger part, or for the most part: *a claim generally recognized*. **2**. usually; commonly; ordinarily: *he*

generally comes at noon. **3**. without reference to particular persons or things: *generally speaking*."[2] It is not clear what would be meant by the appellants' insulative material and conductive element being insulative or conductive with respect to the larger part or for the most part. If "generally" means that the appellants' insulative material and conductive element are usually, commonly or ordinarily insulative or conductive, then it is not clear whether the claim requires the material to be insulative or the element to be conductive. If generally means "without reference to particular persons or things", it is not clear how "generally" limits "insulative material" or "conductive element".

The appellants argue that the meaning of "generally" with respect to the insulative material set forth in their amendment and response filed January 9, 2002 (paper no. 9, page 3) still applies (brief, page 4). That meaning is that the insulative material is not an ideal or perfect insulator. Such nonideality is encompassed by the term "insulating material". It is not clear how "generally" broadens that term.

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[2] *The American College Dictionary* 505 (Random House 1970).

The appellants argue that "generally conductive element" acknowledges the wide variance in conductivity exhibited by various materials (amendment and response filed January 9, 2002, page 3). This argument is not convincing because the term "conductive" encompasses that variation in conductivity. It is not clear from the appellants' disclosure to what extent "generally" broadens that term.

The appellants argue that "'generally insulative material' and 'generally conductive element' include within their scope materials with varying degrees of insulation/conductivity" (brief, page 9). This argument is not well taken because the appellants' disclosure does not indicate the scope of variation encompassed by the term "generally". Moreover, this meaning of "generally" with respect to the insulating material is different than the meaning argued above, i.e., that "generally" indicates deviation from ideality. This inconsistency in the appellants' definitions further indicates the lack of clarity in the term "generally insulative material".

The appellants argue that their specification provides non-limiting embodiments (brief, page 9; amendment and response filed January 9, 2002, page 3). The appellants' disclosure of four exemplary insulative materials (specification, page 5,

lines 24-25), however, does not indicate the degree encompassed by "generally insulative material". Because there are no examples of conductive elements in the specification, there clearly is no indication of the scope encompassed by "generally conductive element".

The appellants argue that a conductor is a material which conducts electricity with ease, and that "generally" is no less definite than "easily" (amendment and response filed January 9, 2002, page 3). This argument is not persuasive because it is unsupported by evidence. Arguments of counsel cannot take the place of evidence. *See In re De Blauwe*, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984).

The appellants argue that because U.S. 5,087,589 to Chapman includes "generally insulative" in claims 20 and 21, and "generally conductive" in claim 21, one of ordinary skill in the art would know the meaning of those terms in the appellants' claim 60 (brief, pages 6-7). This argument is not well taken because Chapman provides in his specification a standard for measuring the degree encompassed by those terms (col. 8, line 67 - col. 9, line 7; col. 10, lines 60-66), whereas the appellants' specification does not provide such a standard.

For the above reasons we conclude that the appellants' claim 60 is indefinite within the meaning of 35 U.S.C. § 112, second paragraph.

Rejections under 35 U.S.C. § 103

Claim 52

Doan discloses a method for processing a semiconductor device (col. 1, lines 6-8), comprising depositing, sequentially, on a semiconductor substrate, a planarization layer (30), a barrier film (40), and a second layer (50) (col. 2, lines 25-44). The barrier film can be an oxide or a nitride (col. 4, lines 17-20), which are among the appellants' barrier layers (specification, page 9, lines 24-33). The second layer can be borophosphosilicate glass (BPSG), which is the appellants' disclosed dielectric layer material (specification, page 7, lines 16-21), and can be tetraethylorthosilicate (TEOS)-based silicate glass (col. 4, lines 38-43). The device then is heated to at least 700°C to reflow the planarization layer and second layer (col. 4, lines 44-51). During this heating the barrier film retains its structural integrity (col. 4, lines 51-53).

The appellants acknowledge the following in their specification:[3]

> It is well known in the art of semiconductor fabrication that dielectric layers formed from organic sources can have shifts in their threshold voltage due to impurities in the dielectric material. The impurities are present in the layer because of the organic processes, such as ozone-TEOS based chemistry, which are used to form the material of the dielectric layer.
>
> It is also known for the impurities in the dielectric layer to diffuse and collect at interfaces close to the substrate during high temperature processing steps performed after deposition of dielectric material formed with organometallic precursors. This diffusion can seriously degrade integrated circuit operation. [page 2, lines 6-20]
>
> * * *
>
> [I]t is known to form the BPSG material of the dielectric layer 20 by reacting ozone with organic precursors such as $(C_2H_5O)_4Si$ (TEOS)[,] triethylphosphate (TEPO) and triethylborane (TEB) in order to provide the required boron, phosphorous, and silicon atoms. Each of these molecules is an organic molecule containing carbon atoms. The contamination due to the carbon of the organic molecules remains in the BPSG dielectric layer 20 after the reactions forming the BPSG material and cause impurities in the BPSG layer 20. [page 7, lines 16-26]

A high temperature processing step used by the appellants which causes impurity diffusion is the step of reflowing the dielectric

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[3] It is axiomatic that our consideration of the prior art must, of necessity, include consideration of the admitted prior art. *See In re Hedges*, 783 F.2d 1038, 1039-40, 228 USPQ 685, 686 (Fed. Cir. 1986); *In re Davis*, 305 F.2d 501, 503, 134 USPQ 256, 258 (CCPA 1962).

layer at 750-1050°C (specification, page 9, lines 4-19). The appellants state that their barrier layer blocks diffusion during the reflow step and/or any other high temperature processing steps (specification, page 9, lines 19-23).

Doan is silent as to the reagents used to form the BPSG. Consequently, one of ordinary skill in the art would have used reagents which were known in the art to be suitable for this purpose such as the above-mentioned TEOS, TEPO and TEB.

The appellants acknowledge in the above-quoted portion of their specification that BPSG formed from TEOS, TEPO and TEB contains carbon as an impurity from each of these reagents, and the appellants disclose that when their dielectric layer is reflowed at 750-1050°C, the impurities in the dielectric layer may diffuse (specification, page 9, lines 4-19). Because Doan's silicate layer reflow temperatures include temperatures above 700°C, it reasonably appears that the impurities (called "electrically chargeable particles" in the appellants' claim 52) in Doan's BPSG or TEOS-based silicate glass dielectric layer, like those in the appellants' dielectric layer, diffuse during the reflow. Because Doan's oxide and nitride barrier layers are made of the same material as the appellants' oxide and nitride barrier layers, it reasonably appears that Doan's barrier layer,

like that of the appellants, prevents the diffusing impurities, to at least some extent, from reaching the substrate.

Doan does not disclose a substrate comprising a plurality of electrically conductive regions and an electrically insulative region therebetween. The examiner argues that in order to provide active areas needed for a working semiconductor surface in Doan, one of ordinary skill in the art would have been led to use, as Doan's semiconductor substrate, a semiconductor substrate such as that shown in Boland's figure 2 having at its surface a plurality of conductive regions (22) with an electrically insulative region (12) therebetween (answer, pages 17-18). There is no dispute as to whether one of ordinary skill in the art would have desired, in Doan's device, active semiconductor surface areas such as those in figure 2 of Boland.

The appellants argue that "one of ordinary skill in the art seeking to planarize layers subsequently provided over Boland's dielectric island/active area surface would turn once again to the CMP [chemical mechanical planarization] method touted by Boland" (brief, page 14). The relevant issue is whether the applied prior art would have led one of ordinary skill in the art to use in Doan's device the semiconductor surface in Boland's figure 2. The appellants have not established that CMP would

provide the reduction in the effects of buckling, also referred to as cracking or wrinkling, which is desired by Doan and is provided by his method (col. 2, lines 21-25). Hence, we are not convinced that one of ordinary skill in the art would not have applied Doan's method to a semiconductor wafer having the working surface shown in figure 2 of Boland.

The appellants argue that "the mechanical aspects of Boland's CMP may very well expose at least one of Doan's layers to stresses having a result similar to one that Doan seeks to avoid" (brief, page 14). The appellants, however, provide no evidence in support of this argument. Arguments of counsel cannot take the place of evidence. *See De Blauwe*, 736 F.2d at 705, 222 USPQ at 196; *In re Payne*, 606 F.2d 303, 315, 203 USPQ 245, 256 (CCPA 1979); *In re Greenfield*, 571 F.2d 1185, 1189, 197 USPQ 227, 230 (CCPA 1978); *In re Pearson*, 494 F.2d 1399, 1405, 181 USPQ 641, 646 (CCPA 1974). Morever, the appellants have provided no evidence that any such stresses would not be overcome by Doan's method for preventing buckling of layers.

The appellants point out that Doan does not mention impurity diffusion, and argue that 1) Doan's TEOS-based silicate glass second layer cannot be assumed to inherently have that impurity diffusion and 2) Doan's oxide or nitride barrier layer cannot be

assumed, merely because Doan discloses these layers structurally, to at least partially prevent the diffused impurities from reaching the substrate (brief, pages 11-13). Doan, however, does not merely disclose a second layer which can be BPSG or a TEOS-based silicate glass, and a barrier layer which can be an oxide or a nitride. Doan also discloses that the device including these layers is heated to at least 700°C sufficiently that the second layer reflows while the barrier layer maintains its structural integrity (col. 4, lines 45-53). Because, as acknowledged by the appellants in the above-quoted portion of their specification, BPSG made using the disclosed known organic reagents contains impurities which may diffuse when the layer is reflowed at 750-1050°C (specification, page 2, lines 6-20 and page 9, lines 6-19), it reasonably appears that the impurities in Doan's BPSG second layer made using those known organic reagents, and the impurities in Doan's TEOS-based silicate glass,[4] likewise may diffuse when the layer is heated to a temperature of at least 700°C sufficient to reflow the layer. *See In re Spada*, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657-58 (Fed. Cir. 1990) ("While Spada

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[4] One of the organic reagents acknowledged in the above-quoted portion of the appellants' specification to be known in the art is TEOS.

criticizes the usage of the word 'appear', we think that it was reasonable for the PTO to infer that the polymerization by both Smith and Spada of identical monomers, employing the same or similar polymerization techniques, would produce polymers having the identical composition.") Also, because Doan's oxide or nitride barrier layer has the same composition as the appellants' oxide or nitride barrier layer, it reasonably appears that it has the property recited in the appellants' claim 52 of preventing at least some of the impurities from reaching the substrate. *See In re Papesch*, 315 F.2d 381, 391, 137 USPQ 43, 51 (CCPA 1963)("From the standpoint of patent law, a compound and all of its properties are inseparable; they are one and the same thing.") "[W]hen the PTO shows sound basis for believing that the products of the applicant and the prior art are the same, the applicant has the burden of showing that they are not." *See Spada*, 911 F.2d at 708, 15 USPQ2d at 1658. Whether a rejection is under 35 U.S.C. § 102 or § 103, when the appellants' product and that of the prior art appear to be identical or substantially identical, the burden shifts to the appellants to provide evidence that the prior art product does not necessarily or inherently possess the relied-upon characteristics of the appellants' claimed product. *See In re Fitzgerald*, 619 F.2d 67,

70, 205 USPQ 594, 596 (CCPA 1980); *In re Best*, 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977); *In re Fessmann*, 489 F.2d 742, 745, 180 USPQ 324, 326 (CCPA 1974). The reason is that the Patent and Trademark Office is not able to manufacture and compare products. *See Best*, 562 F.2d at 1255, 195 USPQ at 434; *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972). The appellants have not carried that burden.

For the above reasons we conclude that a *prima facie* case of obviousness of the method claimed in the appellants' claim 52 has been established and has not been effectively rebutted by the appellants. Accordingly, we affirm the rejection of that claim.

Claim 53

Doan discloses a method for processing a semiconductor device, comprising forming, sequentially, a planarization layer (30), a barrier layer (40), and a BPSG or TEOS-based silicate glass dielectric layer (50), on a substrate, and then heating the device to reflow the planarization layer and the dielectric layer while the barrier layer maintains its structural integrity (col. 2, lines 21-50; col. 3, lines 50-59; col. 4, lines 17-53). As discussed above regarding the rejection of claim 52, it reasonably appears that 1) during the reflow step, impurities, called electrically chargeable particles in the

appellants' claim 53, deposit in the dielectric layer and diffuse within that layer, and 2) the barrier layer prevents at least some of the impurities from reaching the substrate. The appellants acknowledge that carbon is an impurity from TEOS and from the TEPO and TEB used together with TEOS to form BPSG (specification, page 7, lines 3-5 and 16-29). Carbon apparently is what the appellants refer to in their claim 53 as an organic component of the organic precursor.

Doan is silent as to the precursor used to form the oxide or nitride barrier layer. One of ordinary skill in the art, therefore, would have used any precursor known in the semiconductor art to be suitable for making oxide or nitride layers. Such precursors for making silicon nitride include silane and nitrogen as taught by Cunningham (abstract).

The appellants argue that the examiner, in focusing upon only the portion of Cunningham pertaining to formation of a silicon nitride film, improperly relies upon guidance from the appellants' specification (brief, page 18). This argument is not well taken because the use of silane and nitrogen-containing and oxygen-containing precursors for making silicon nitride and silicon oxide films was very well known to those of ordinary skill in the semiconductor art at the time of the appellants'

invention.[5] Hence, regardless of Cunningham's other disclosure, Cunningham's disclosure pertaining to the formation of a silicon nitride barrier layer would have fairly suggested, to one of ordinary skill in the art, silane and nitrogen as the precursors for forming Doan's silicon nitride barrier layer.

We therefore affirm the rejection of claim 53 and claims 54-57 that stand or fall therewith.

Claim 59

Doan discloses a method for forming a circuit device, comprising providing a semiconductor substrate, layering a barrier on the substrate, layering a dielectric on the barrier, and then heating the device to at least 700°C to reflow the dielectric layer while the barrier layer maintains its structural integrity (col. 2, lines 21-50; col. 3, lines 50-59; col. 4, lines 17-53). As discussed above regarding the rejection of claim 52, Doan's BPSG and TEOS-based silicate glass are carbon-containing dielectrics. As for the requirement that the barrier is carbon free, Doan does not disclose that his nitride and oxide barrier films contain carbon (col. 4, lines 17-19). Moreover, as

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[5] *See, e.g.*, 10 *Kirk-Othmer Encyclopedia of Chemical Technology* 266-67 (John Wiley & Sons, 3rd ed. 1980) and 13 *Kirk Othmer* at 639-640 (1981), copies of which are provided to the appellants with this decision.

discussed above with respect to claim 53, the applied prior art would have fairly suggested, to one of ordinary skill in the art, making Doan's barrier film from a non-organic precursor.

Doan does not disclose that "at least 700°C" includes 750°C, and is silent as to the reflow time. However, because the material reflowed can be BPSG, which is the appellants' disclosed dielectric layer material (specification, page 7, lines 16-20; page 9, lines 4-10), it reasonably appears that the workable reflow temperatures of at least 700°C and reflow times, determined by one of ordinary skill in the art through no more than routine experimentation, would include those used by the appellants, i.e., temperatures including 750°C and times including 5 minutes. *See In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Moreover, Ying teaches that BPSG can be reflowed at 700-900°C for approximately 5-120 minutes (col. 4, lines 17-20). This teaching would have led one of ordinary skill in the art to use, as Doan's temperature of at least 700°C, any temperature in the 700-900°C range, including 750°C, and to use any reflow time in the range of approximately 5-120 minutes.

The appellants argue that one of ordinary skill in the art would not have combined the teachings of Doan and Ying because Doan desires to reduce the stress resulting from buckling,

whereas Ying reflows his BPSG in an active ambient to create internal stress which aids in planarization (col. 4, lines 9-13) (brief, pages 20-23). Ying, however, does not indicate that the required reflow temperature and time depend on the ambient. Hence, one of ordinary skill in the art would have been led by Doan and Ying to use Ying's reflow temperatures and times, in the absence of the stress-forming active ambient, when reflowing Doan's BPSG.

The appellants argue that Ying teaches against high temperatures, particularly temperatures above 900°C, because they cause degradation of the underlying semiconductor device (brief, page 21). This teaching by Ying would have fairly suggested, to one of ordinary skill in the art, using, as Doan's BPSG reflow temperature of at least 700°C, any temperature within the 700-900°C range, including temperatures of 750-900°C which are within the scope of the appellants' claim 59, in order to avoid degrading the underlying semiconductor device.

For the above reasons we affirm the rejection of claim 59 and claim 58 that stands or falls therewith.

Claims 60-64

We need to address only claim 60, which is the sole independent claim among claims 60-64.[6]

The appellants' claim 60 requires that a generally conductive element is generally laterally coextensive with an intervening insulating region.

As discussed above regarding the rejection under 35 U.S.C. § 112, second paragraph, the terms "generally insulative material" and "generally conductive element" render the appellants' claim 60 indefinite. However, regardless of the meaning of those terms, because the appellants' figure 1 provides some standard for measuring the degree encompassed by "generally laterally coextensive", we are able to determine whether the examiner has established a *prima facie* case of obviousness of a substrate processing method including this limitation. In the interest of judicial economy, we make that determination. *See Ex parte Saceman*, 27 USPQ2d 1472, 1474 (Bd. Pat. App. & Int. 1993); *Ex parte Ionescu*, 222 USPQ 537, 540 (Bd. App. 1984).

[6] The examiner does not rely upon Van Der Scheer for any disclosure that remedies the deficiency in Doan and Ghezzi as to claim 60.

The ordinary meaning of "coextensive" is "[h]aving the same limits, boundaries, or scope."[7] The appellants' figure 1 is consistent with this meaning with respect to lead 26 and insulating region 14, i.e., it shows them as having essentially the same lateral dimension.

The examiner argues that Ghezzi discloses "providing a generally conductive element (5) over a generally insulative material (21), wherein the element is generally laterally coextensive with the intervening insulating region" (answer, page 9).[8] As shown in Ghezzi's figure 3, however, floating gate 5 extends far beyond gate oxide 21. Thus, based upon any reasonable interpretation of "generally laterally coextensive" in view of the appellants' figure 1, these layers are not generally laterally coextensive. The examiner argues that "the Appellant has not explained why the generally conductive layer is not allowed to extend over another feature of a structure while still

[7] *Webster's II New Riverside University Dictionary* 278 (Riverside 1984).

[8] The examiner also argues that "[t]he issue is whether the generally conductive layer (22) is generally laterally coextensive with the generally insulating region (21) in figure 3 of Ghezzi" (answer, page 24). Ghezzi's item 22 is not identified, but it appears to be comparable to item 24 (figure 3), i.e., an area of floating gate 5.

being generally laterally coextensive with the generally insulating region" (answer, page 24). The reason is that if the conductive layer extends over another feature, it is not generally laterally coextensive with the insulating region according to any reasonable meaning of "generally laterally coextensive" indicated by the appellants' figure 1.

Accordingly, we reverse the rejections of claims 60-64 under 35 U.S.C. § 103.

OTHER ISSUE

In the event of further prosecution the examiner should consider rejecting claims 61-64 under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which the appellants regard as the invention. Claims 61-64 include the subject matter of claim 60 from which they directly or indirectly depend. As discussed above regarding the rejection under 35 U.S.C. § 112, second paragraph, "generally insulative material" and "generally conductive element" in claim 60 are indefinite. Claims 61-64 do not remedy the lack of clarity of these terms in claim 60. Consequently, claims 61-64 are indefinite.

DECISION

The rejection of claim 60 under 35 U.S.C. § 112, second paragraph, and the rejections under 35 U.S.C. § 103 of claim 52 over Doan in view of Boland, claims 53-57 over Doan in view of Cunningham, and claims 58 and 59 over Doan in view of Cunningham and Ying, are affirmed. The rejections under 35 U.S.C. § 103 of claims 60, 61, 63 and 64 over Doan in view of Ghezzi, and claim 62 over Doan in view of Ghezzi and Van Der Scheer, are reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

Terry J. Owens
TERRY J. OWENS
Administrative Patent Judge

Thomas A. Waltz
THOMAS A. WALTZ
Administrative Patent Judge

Paul Lieberman
PAUL LIEBERMAN
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

TJO/ki

Charles Brantley
Micron Technology, Inc.
8000 S. Federal Way
Mail Stop 525
Bosie, ID 83716

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Chemical Vapor Deposition (Cvd). Chemical vapor deposition (cvd), also called vapor plating or vapor forming, is a process in which a surface is coated with vapors of volatile stable chemical compounds at a temperature below the melting point of the surface. The compound is reduced or dissociated (69–72), resulting in an adherent coating of material. An example of this process is titanium vapor plating by the reduction of titanium tetrabromide with hydrogen at an elevated temperature. Solid $TiBr_4$ is vaporized and the vapor mixed with hydrogen. The mixture is conducted over the surface which is heated to about 1300°C. There it decomposes, depositing a coating of titanium metal.

In another variation of this technique, nickel carbonyl vapor is passed over a mandrel in a closed chamber at ca 175°C. Upon contacting the mandrel surface, the nickel carbonyl decomposes into nickel and carbon monoxide. A minute amount of nickel is deposited, and the carbon monoxide vapors are recirculated, yielding a controlled growth of nickel at a rate of 0.025 mm/h. This produces a uniform precise nickel coating on the mandrel without additional buildup on edges or projections and has proven commercially useful for preparation of nickel shells and molds.

The cvd technique is also applicable to the decomposition of surface coating of refractory metals and compounds such as the carbides of tantalum and silicon, tin oxide, and carbon. The advantages of the process include deposition of coatings varying from the ultrathin up to a thickness of many millimeters; the main disadvantage is the necessity of heating the surface to be coated.

Commercially, cvd is used to produce epitaxially grown single crystal silicon by the reduction of silicon tetrachloride with hydrogen and to make epitaxial compounds, polysilicon, silicon nitride, silicon dioxide, and both doped polysilicon and silicon dioxide. Each coating can be deposited ideally in a selected temperature range (73) as shown in Table 1.

Several different types of equipment have evolved to meet select requirements of chemical vapor deposition. Among them are horizontal, vertical, cylindrical, tubular, cold-wall, and hot-wall systems. In the horizontal system, the stationary silicon wafers are processed lying flat or on a moving belt in a continuous process furnace. The vertical reactor employs a bell jar in which wafers are placed on a susceptor disk and rotate continually for uniform coverage. In the cylindrical reactor the wafers are peripherally mounted. The tubular system configuration is similar to the horizontal type with multitiered carriers being used. A typical low pressure cvd configuration is shown in Figure 12.

Table 1. Typical Deposition Reactions—Atmospheric Pressure Cvd Reactors

Film	Carrier gas	Reaction	Deposition temperature range (°C)
Si_3 epitaxy	H_2	$SiCl_4 + H_2 \rightarrow Si + HCl$	1125–1200
Si_3 epitaxy	H_2	SiH_4 + heat $\rightarrow Si + H_2$	1000–1075
Si_3N_4	H_2	$SiH_4 + NH_3 \rightarrow Si_3N_4 + H_2$	900–1100
poly Si	H_2	$SiH_4 + NH_3 \rightarrow Si_3N_4 + H_2$	600–700
poly Si	H_2	SiH_4 + heat $\rightarrow Si + H_2$	850–1100
SiO_2	H_2	$SiH_4 + CO_2 \rightarrow SiO_2 + H_2 + CO$	600–900
SiO_2	H_2	$SiH_4 + CO_2 \rightarrow SiO_2 + CO$	500–900
SiO_2	H_2	$SiCl_4 + CO_2 \rightarrow SiO_2$	800–1000
SiO_2	H_2	$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$	200–500

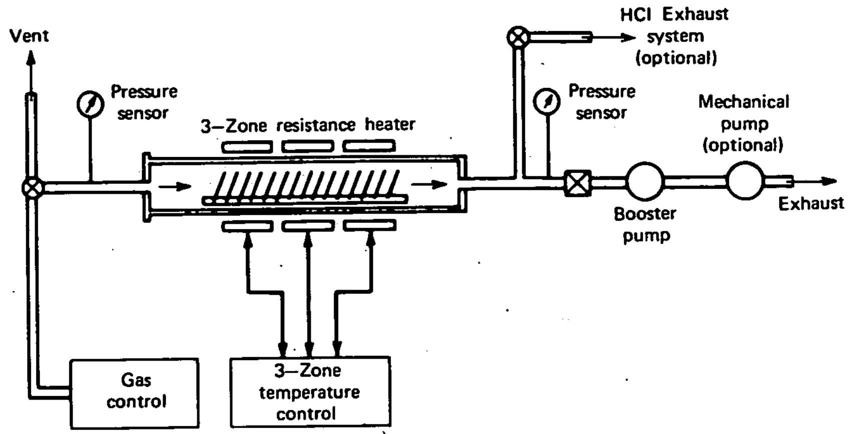

Figure 12. Typical low-pressure cvd configuration.

Two types of systems are used for heating the equipment. The cold-wall system contains either an external r-f induction coil that couples energy through the quartz chamber wall to the susceptor which in turn heats the wafers, or an external radiant heater in contact with the clear quartz wall of the chamber. In the hot-wall system the outside of the chamber wall is wrapped with resistance heaters which heat the wafers through internal-directed radiation.

Other commercial uses of chemical vapor deposition are deposition of carbon thin films by pyrolytic decomposition of organic materials and manufacture of capacitors of titanium dioxide with dielectric constants as high as 82. These capacitors are produced by the hydrolysis of titanium tetrachloride.

Electron-Beam Polymerization. Electron beams can provide the necessary energy to cause polymerization of organic monomers. Monomeric materials that have been irradiated to produce films include silicones (74), butadiene (75), styrene (76), methyl methacrylate (77), divinylbenzene (78), and epoxy resins (79–80). However, the lack of selectivity of this energy source results in formation of unwanted contaminant materials (81–82) (see Radiation curing).

Film properties can be tailored somewhat by varying the voltage used to accelerate the electrons. The lower the voltage, the less cross-linked and softer the polymer film. Use of voltages greater than 1000 V cause crazing of films owing to excessive cross-linking. Typical growth rates are ca 0.5 μm/h.

Electron-beam polymerization, like ultraviolet polymerization, is useful for forming films without a mask (80). It is capable of yielding film pattern resolution as low as 1 μm. Film patterns can be obtained by irradiating a large surface area with a defocused electron beam or by scanning with a small electron beam.

Gamma Radiation. Gamma radiation can be used for formation of thin polymeric films via a mechanism of free-radical polymerization similar to that occurring in ultraviolet and electron-beam polymerization. The condensation polymerization reactions effected by gamma irradiation can be as specific as most chemical reactions because the initial energy is rapidly degraded in matter and much of the chemical change produced by radiation is a consequence of the action of electrons of less than 100 eV. The transient species produced by such electrons do not give final products immediately, but take part in various transfer processes in such a way that the molecules finally transformed to products are not necessarily the ones that were initially affected.

KIRK-OTHMER

ENCYCLOPEDIA OF CHEMICAL TECHNOLOGY

THIRD EDITION

VOLUME 13

HYDROGEN-ION ACTIVITY
TO
LAMINATED MATERIALS, GLASS

1981

A WILEY-INTERSCIENCE PUBLICATION
John Wiley & Sons
NEW YORK • CHICHESTER • BRISBANE • TORONTO

that is used for generating the plasma in sputtering is replaced by a gas that reacts with the material that is to be deposited or etched (52). If titanium or silicon are sputtered in a nitrogen atmosphere, then under the proper plasma conditions, titanium nitride, a metal, or silicon nitride (as an insulator) can be deposited. Similarly, for etching, if a gas is used that reacts with the material to be etched and forms volatile compounds, then higher etch rates and/or higher selectivity with respect to other materials may be obtained.

Plasma Deposition and Etching. Plasma-assisted deposition and etching are processes in which the function of the plasma is to generate reactive chemical species and which generally are carried out in a parallel-plate radial-flow reactor, as shown in Figure 11 (54–55). This reactor design provides the uniformity and the temperature and plasma control that are necessary for IC fabrication, and it has become the standard for critical deposition and etching processes.

Plasma etching processes have been developed for most thin films that are used in IC fabrication; a list of materials, etch gases, and typical etch rates are given in Table 3.

Establishing an adequate etch selectivity between the material being etched and underlying layers can be a problem with plasma etching (58). For thermally grown, silicon dioxide layers, the etch selectivity with respect to silicon using wet chemical etching, eg, hydrofluoric acid, is infinite, whereas with plasma etching, the best selectivities that have been reported are ≤ 15.

Plasma-assisted deposition has been used to deposit silicon dioxide, silicon nitride, and polycrystalline silicon (59). The most widely used material is plasma-deposited silicon nitride which is deposited from a mixture of silane, ammonia, and argon and/or nitrogen at temperatures from 300–350°C and which is used as a metallization overcoat and an insulating layer in multilevel metal structures (60). The salient feature of

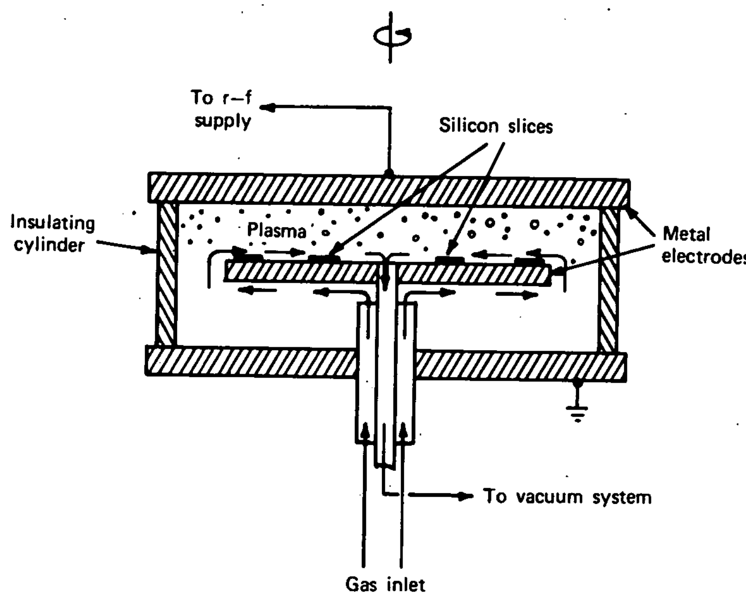

Figure 11. Horizontal parallel-plate radial-flow plasma reactor.

Table 3. Plasma Etch Gases for IC Materials[a]

Material	Etch gas	Typical etch rates, nm/min
thermal SiO_2	CF_4–O_2	10
	C_2F_6–CF_3Cl	30
	C_2F_6–CHF_3	70
phosphosilicate glass	C_2F_6–CHF_3	120
	C_2F_6–CF_3Cl	30
Si_3N_4	CF_4–O_2	70
	C_2F_6–CF_3Cl	30
	C_2F_6–CHF_3	70
plasma-deposited SiN	CF_4–O_2	150–300
	C_2F_6–CF_3Cl	50
	C_2F_6–CHF_3	70
single-crystal Si	CF_4–O_2	100
	C_2F_6–CF_3Cl	90
	C_2F_6–CHF_3	10
vapor-deposited poly-Si	C_2F_6–CHF_3	15
	C_2F_6–CF_3Cl	100
aluminum	CCl_4–Ar–H_2	100
	CCl_4–Cl_2	100

[a] Refs. 56 and 57.

plasma deposition is that, at low deposition temperatures (<400°C), it provides films with properties that usually are obtained only at much higher temperatures, eg, plasma silicon nitride provides excellent coverage over harsh topology.

Metallization. Metallization provides contact to the silicon and interconnects devices. Silicon contact is made at windows that are etched in a final glass layer which is formed over the entire wafer, either by thermal oxidation or vapor deposition, after all impurity regions have been defined. The metal is deposited uniformly and then patterned, the pattern being determined by the circuit function.

Aluminum is the most widely used metallization (61) and, for MOS ICs, it is predominant. For bipolar, two systems are used: one is based on aluminum but is modified to meet unique bipolar requirements (62) and the other is based on gold (63). The most commonly used IC metal systems are described in Table 4 and sheet resistances and typical thicknesses of the materials are given in Table 5 (see Electrical connectors).

Table 4. IC Metal Systems

MOS ICs	Bipolar ICs			Material function
Al, poly-Si	PtSi	PtSi	*1st Level*	Si contact
		Ti		glue layer
	Ti, W	TiN		barrier layer
poly-Si	Al	Pt		interconnection I
SiO_2 (P-doped)	SiO_2 (P-doped)	SiN		interlevel dielectric
SiO_2				
		Ti	*2nd Level*	glue layer
	Ti, W	TiN, Pt		barrier layer
Al	Al	Au		interconnection II